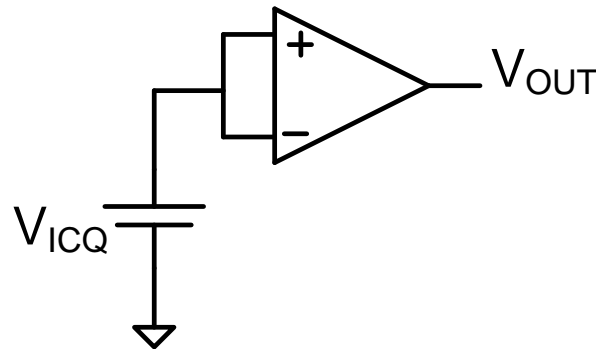# EE 435

Lecture 22

Offset Voltages

Offset Voltage

Two types of offset voltage:

- Systematic Offset Voltage
- Random Offset Voltage

Definition: The output offset voltage is the difference between the desired output and the actual output when $V_{id}=0$ and V_{ic} is the quiescent common-mode input voltage.

$$V_{OUTOFF} = V_{OUT} - V_{OUTDES}$$

Note: V_{OUTOFF} is dependent upon V_{ICQ} although this dependence is usually quite weak and often not specified

Offset Voltage
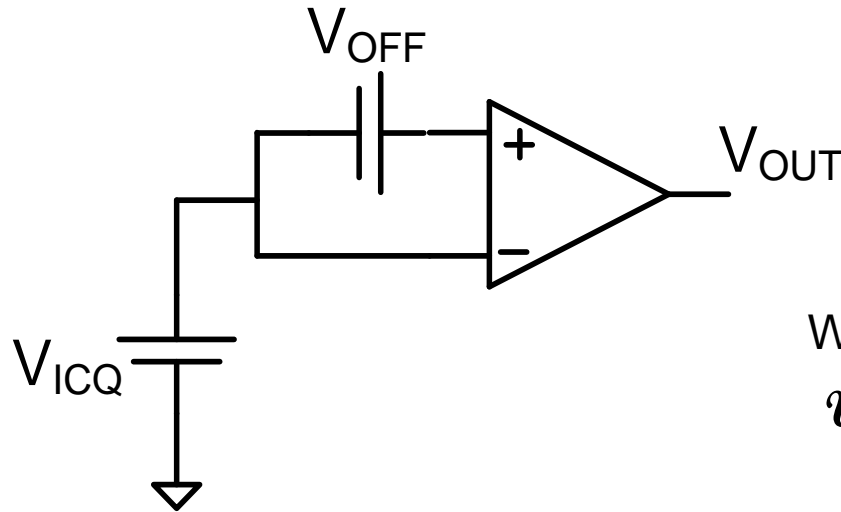
When operating linearly

$$v_{OUT} = A_D v_D + A_C v_C$$

Definition: The input-referred offset voltage is the differential dc input voltage that must be applied to obtain the desired output when V_{ic} is the quiescent common-mode input voltage.

V_{OFF} is usually related to the output offset voltage by the expression

$$V_{OFF} = \frac{V_{OUTOFF}}{A_D}$$

V_{OFF} is dependent upon V_{ICQ} although this dependence is usually quite weak and often not specified

V_{OFF} almost always large enough to force open-loop op amp out of linear mode for good op amps

Offset Voltage

Note: Our definition differs from that of most others

From Wikipedia March 3, 2024

The **input offset voltage** (V_{os}) is a parameter defining the differential DC voltage required between the inputs of an amplifier, especially an operational amplifier (op-amp), to make the output zero (for voltage amplifiers, 0 volts with respect to ground or between differential outputs, depending on the output type).[1]

From Analog Devices   MT-037 Tutorial

Ideally, if both inputs of an op amp are at exactly the same voltage, then the output should be at zero volts. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the input offset voltage, V_{OS}

Offset Voltage: The differential voltage which must be applied to the input of an op amp to produce zero output.

Offset Voltage

Note: Our definition differs from that of most others

From Texas Instruments Application Note: SLOA059 – March 2001

Input Offset Voltage Defined

The input offset voltage is defined as the voltage that must be applied between the two input terminals of the op amp to obtain zero volts at the output. Ideally the output of the op amp should be at zero volts when the inputs are grounded.
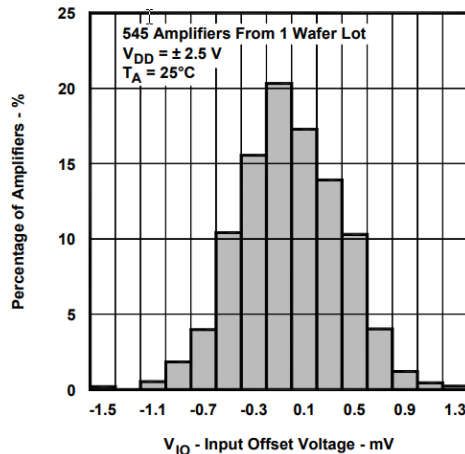

Figure 3.   Distribution of V_{IO} for the TLV2721

Implicit in the definition of V_{OS} by most others is that the desired output voltage of an op amp is 0v when the differential input is 0V

Offset Voltage

Note: Our definition differs from that of most others

Implicit in the definition of V_{OS} by most others is that the desired output voltage of an op amp is 0v when the differential input is 0V

Note: Difference in definition of offset is usually insignificant once an op amp has been designed

So, if difference in definition of offset is insignificant, is there any reason to define it differently and to emphasize the difference or emphasize that there is no significant difference?

- Pointing out difference may simplify analytical formulation of offset

- Emphasize using a Degree of Freedom to achieve target offset voltage is typically not justifiable

Offset Voltage

From Analog Devices   MT-037 Tutorial

◆ **Ranges:**
- **Chopper Stabilized Op Amps:**   **<1µV**
- **General Purpose Precision Op Amps:**   **50-500µV**
- **Best Bipolar Op Amps:**   **10-25µV**
- **Best JFET Input Op Amps:**   **100-1,000µV**
- **High Speed Op Amps:**   **100-2,000µV**
- **Untrimmed CMOS Op Amps:**   **5,000-50,000µV**
- **DigiTrim™ CMOS Op Amps:**   **<100µV-1,000µV**

Figure 1: Typical Op Amp Input Offset Voltage

These ranges probably are applicable to catalog op amps

Offset Voltage

From Analog Devices   MT-037 Tutorial

INPUT OFFSET VOLTAGE DRIFT AND AGING EFFECTS

Input offset voltage varies with temperature, and its temperature coefficient is known as *TCVos*, or more commonly, *drift*. Offset drift is affected by offset adjustments to the op amp, but when the offset voltage of a bipolar input op amp has been minimized, the drift may be as low as 0.1 µV/°C (typical value for OP177F). More typical drift values for a range of general purpose precision op amps lie in the range 1-10 µV/°C. Most op amps have a specified value of TCVos, but some, instead, have a second value of maximum Vos that is guaranteed over the operating temperature range. Such a specification is less useful, because there is no guarantee that TCVos is constant or monotonic.

The offset voltage also changes as time passes, or *ages*. Aging is generally specified in µV/month or µV/1000 hours, but this can be misleading. Since aging is a "drunkard's walk" phenomenon, it is proportional to the *square root* of the elapsed time. An aging rate of 1 µV/1000 hour therefore becomes about 3 µV/year (not 9 µV/year).

Offset Voltage

Two types of offset voltage:

- Systematic Offset Voltage
- Random Offset Voltage
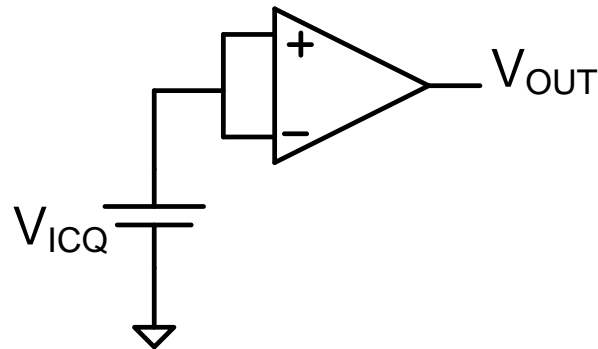
After fabrication it is impossible (difficult) to distinguish between the systematic offset and the random offset in any individual op amp

Measurements of offset voltages for a large number of devices will provide mechanism for identifying systematic offset and statistical characteristics of the random offset voltage

Systematic Offset Voltage

Offset voltage that is present if all device and model parameters assume their nominal value

Easy to simulate the systematic offset voltage

Almost always the designer's responsibility to make systematic offset voltage very small

Generally easy to make the systematic offset voltage small

Random Offset Voltage

- Due to random variations in process parameters and device dimensions

- Random offset is actually a random variable at the design level but deterministic after fabrication in any specific device

- Distribution naturally nearly Gaussian (could be un-naturally manipulated)

    Has zero mean

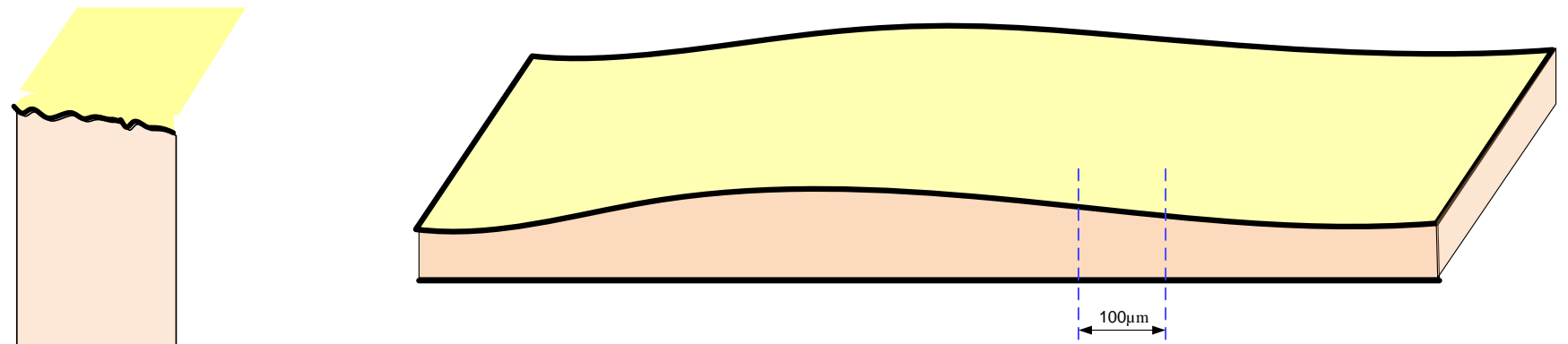   Characterized by its standard deviation or variance

    Often strongly layout dependent

    Due to both local random variations and correlated gradient effects

    - o Will consider both effects separately
    - o Gradient effects usually dominate if not managed
    - o Good methods exist for driving gradient effects to small levels

Gradient and Local Random Effect

100μm

Gradient Effects : Locally Appear Linear

- Magnitude and Direction of Gradients are random
- Highly Correlated over Short Distances

0.01μm

Local Random Effects :
Vary Locally With No
Correlation

- **Both Contribute to Offset**
- **Both are random variables**
- **If Not Managed, Both Can Cause Large Offsets**
- **Strategies for minimizing their effects are different**
- **Will refer to the local random effects as "random" and the random gradient effects as "gradient" effects**
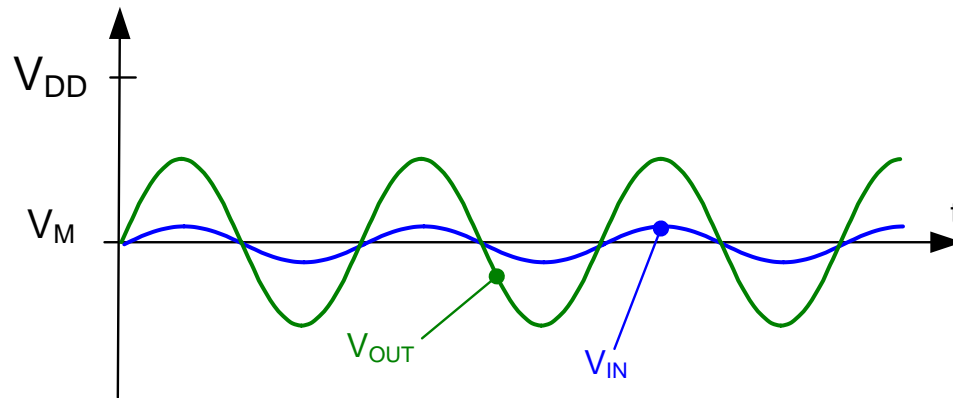
Offset Voltage
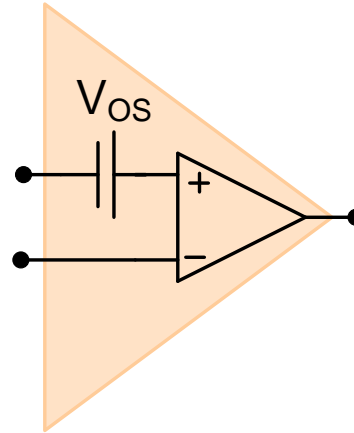
Can be modeled as a dc voltage source in series with the input

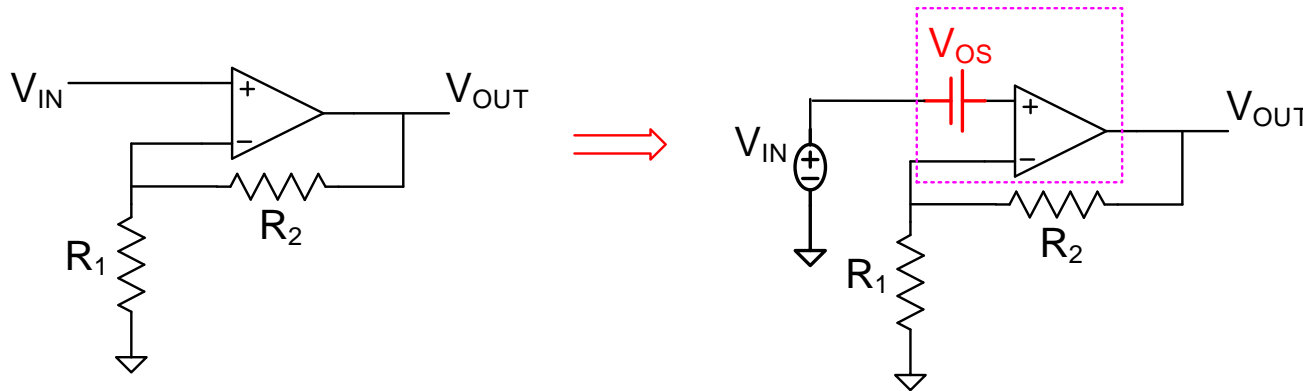# Offset Voltage

Effects of Offset Voltage - <u>an example</u>

V_{IN} ▷+ V_{OUT} ▷− R_2 R_1

Desired I/O relationship

V_{DD}

V_M

t

V_{OUT}

V_{IN}
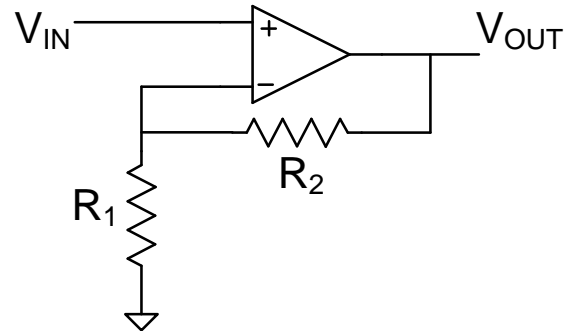
Offset Voltage

Effects of Offset Voltage - <u>an example</u>

By Superposition:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) V_{IN} + \left(1 + \frac{R_2}{R_1}\right) V_{OS}$$
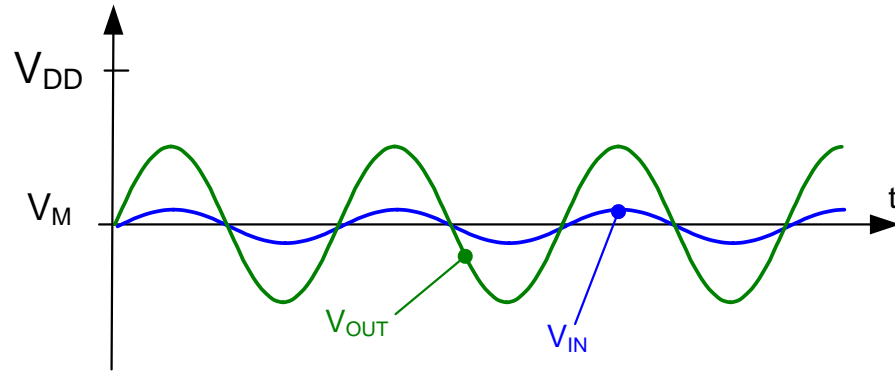
In this feedback circuit, V_{OS} multiplied by same gain as V_{IN}

Particularly problematic if V_{IN} is small (so FB gain is then usually large)
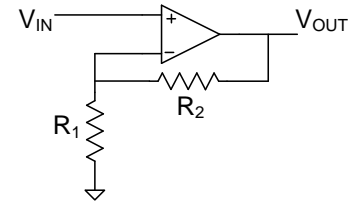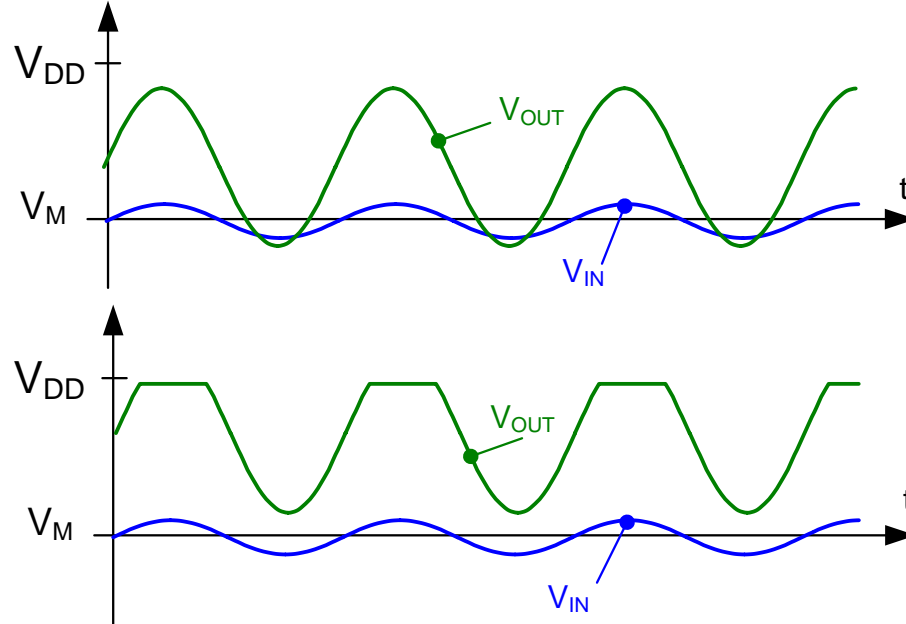
Offset Voltage

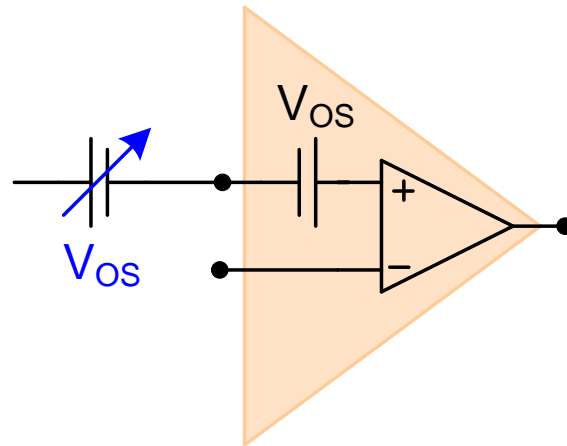Effects of Offset Voltage - <u>an example</u>

Desired I/O relationship

Actual I/O relationship due to offset

Offset Voltage

Effects can be reduced or eliminated by adding equal amplitude opposite DC signal (many ways to do this)

Widely used in offset-critical applications

Comes at considerable effort and expense for low offset

Prefer to have designer make V_{OS} small in the first place
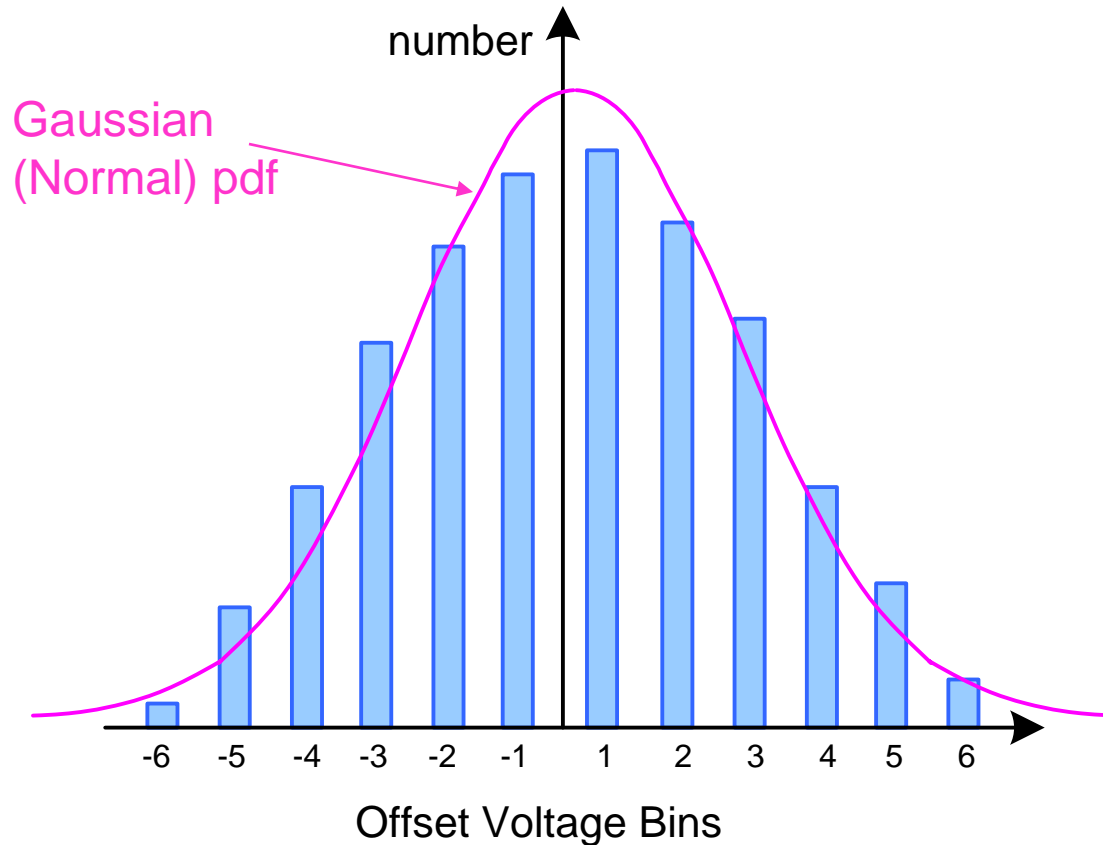
Effects of Offset Voltage

• Deviations in performance will change from one instantiation to another due to the random component of the offset

• Particularly problematic in circuits with high FB gain

• A major problem in many other applications

• Not of concern in many applications as well

Random Offset Voltage Distribution
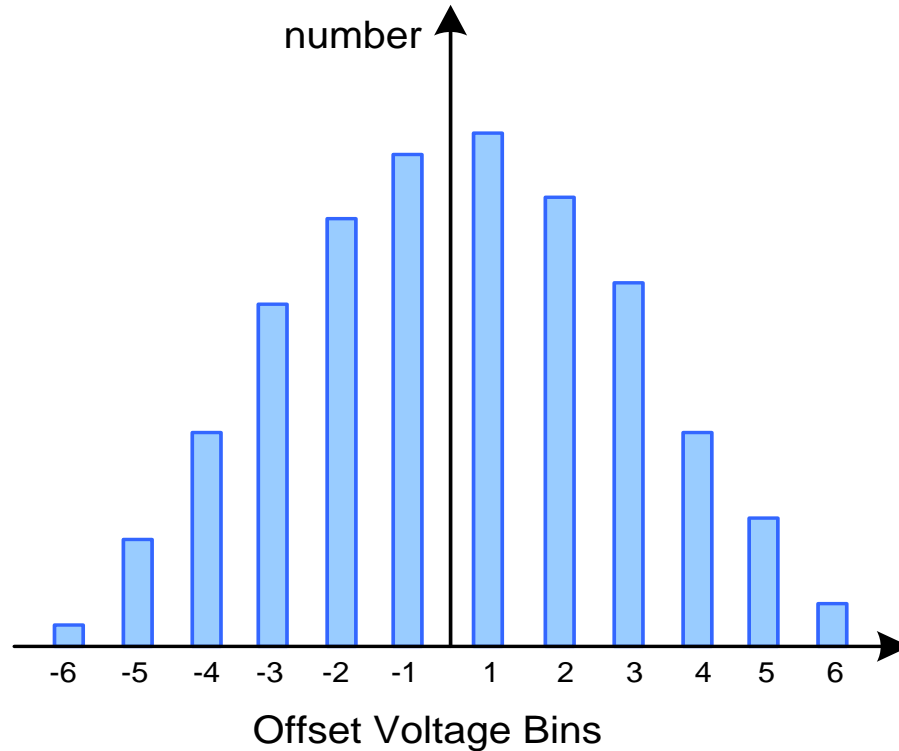
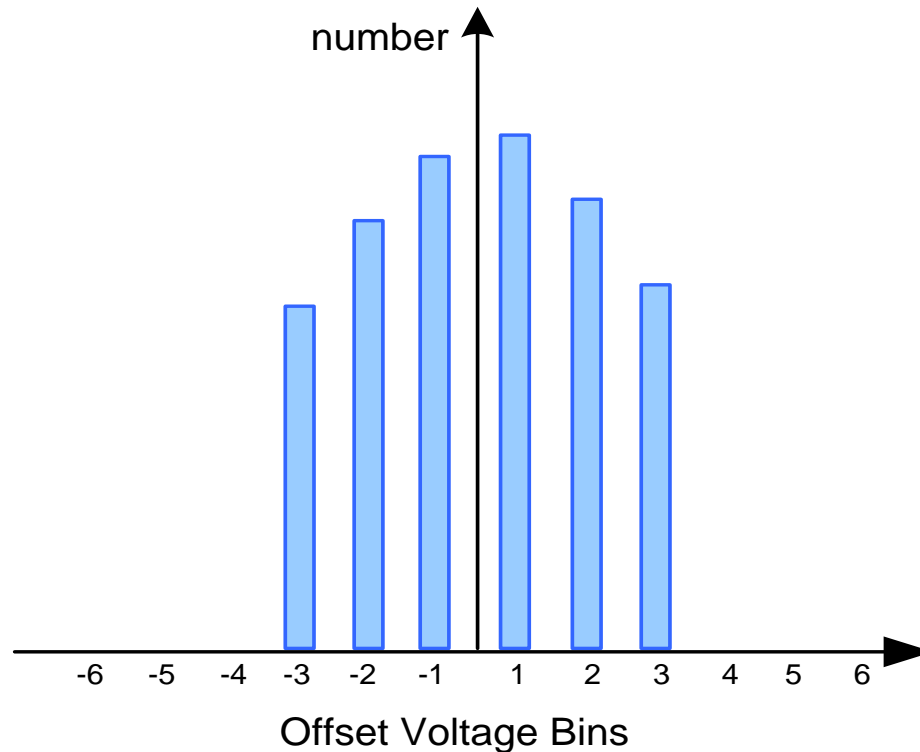Typical histogram of random offset voltage (binned) after fabrication

Random Offset Voltage Distribution

Typical histogram of offset voltage (binned) after fabrication

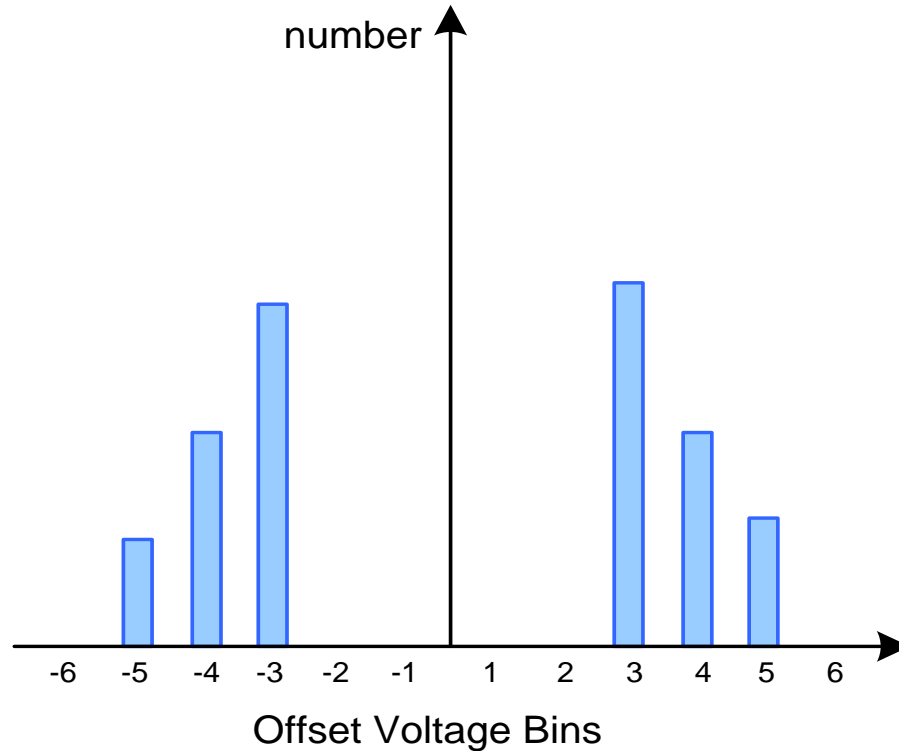Mean is nearly 0 (mean is actually the systematic offset voltage)

Random Offset Voltage Distribution

Typical histogram of offset voltage (binned) in shipped parts

Extreme offset parts have been sifted at test

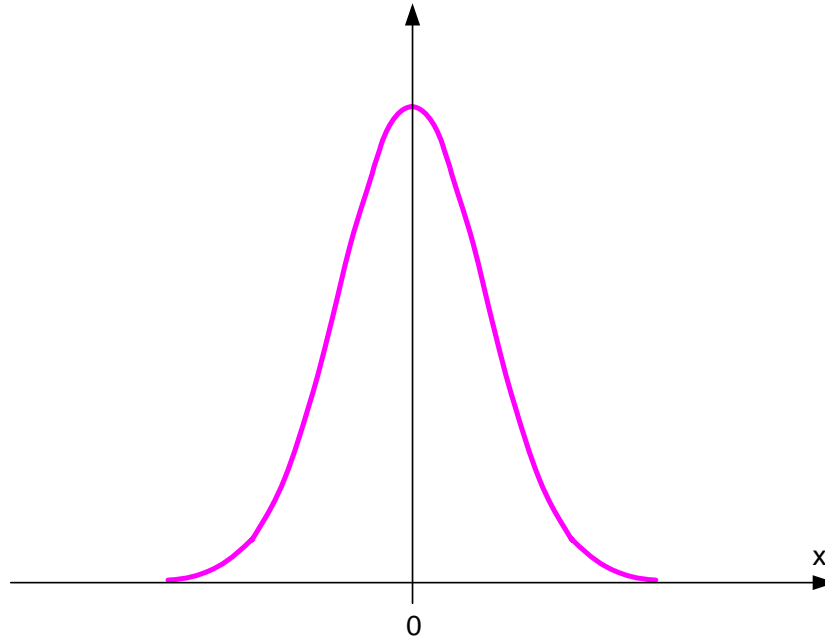# Random Offset Voltage Distribution

Typical histogram of offset voltage (binned) in shipped parts

Low-offset parts sometimes sold at a premium

Extreme offset parts have been sifted at test

Random Offset Voltage Distribution

Pdf of zero-mean Gaussian distribution

Characterized by its standard deviation σ or variance σ^2

Offset voltage often specified as the 1σ or 3σ value (though authors may neglect to indicate which)

For catalog parts, often specified as the worst-case value after test sort

Random Offset Voltage Distribution

Pdf of zero-mean Gaussian distribution
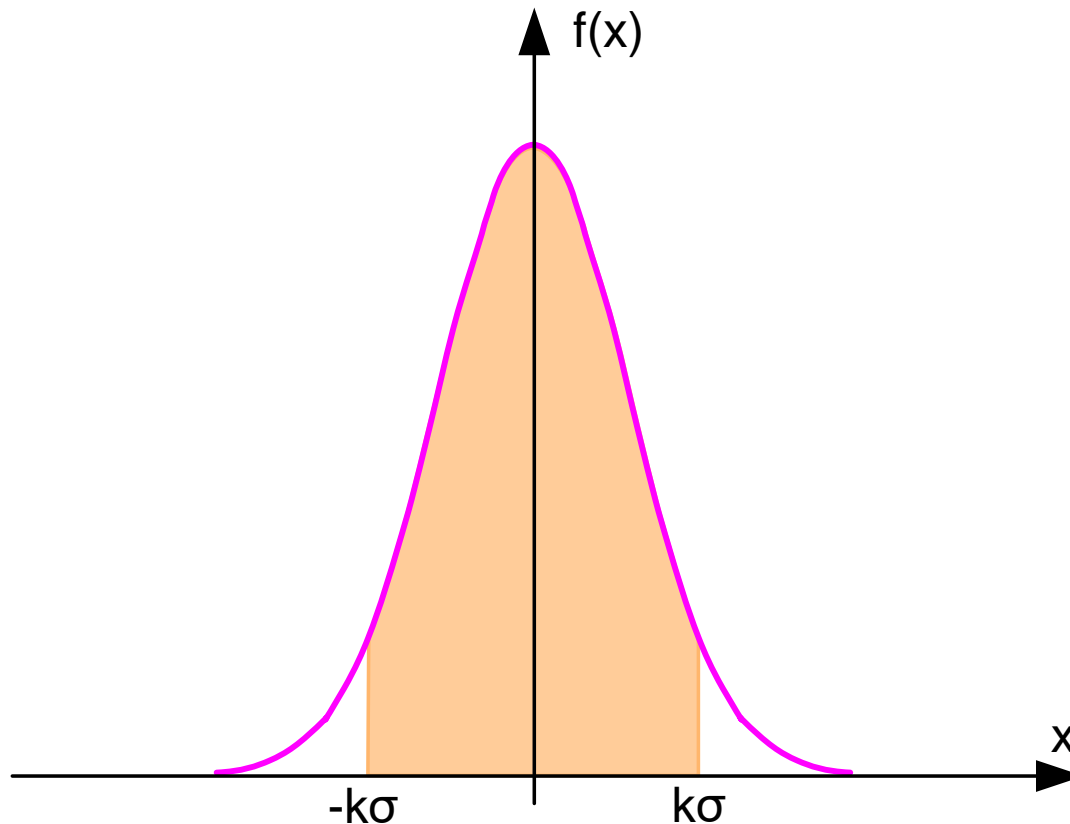
Percent between:		
	$\pm\sigma$	68.3%
	$\pm2\sigma$	95.5%
	$\pm3\sigma$	99.73%

Offset Voltage

TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

Check for Samples: TL082-N

FEATURES

- **Internally Trimmed Offset Voltage: 15 mV**
- **Low Input Bias Current: 50 pA**
- **Low Input Noise Voltage: 16nV/√Hz**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **Wide Gain Bandwidth: 4 MHz**
- **High Slew Rate: 13 V/μs**
- **Low Supply Current: 3.6 mA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Total Harmonic Distortion: ≤0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 2 μs**

DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input

DC Electrical Characteristics [1]

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10$ kΩ, $T_A = 25$°C		5	15	mV
		Over Temperature			20	mV

Sifted at test if $|V_{OFF}|>15\text{mV}$

Guess 3σ value of trimmed but non-culled population is 15 mV
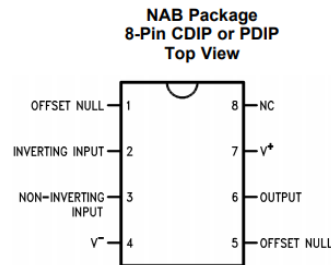
Offset Voltage

LM741 Operational Amplifier

1 Features

- Overload Protection on the Input and Output
- No Latch-Up When the Common-Mode Range is Exceeded

2 Applications

3 Description

The LM741 series are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

NAB Package
8-Pin CDIP or PDIP
Top View

OFFSET NULL — 1		8 — NC
INVERTING INPUT — 2		7 — V$^+$
NON−INVERTING INPUT — 3		6 — OUTPUT
V$^-$ — 4		5 — OFFSET NULL

6.5 Electrical Characteristics, LM741[1]

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \leq 10$ kΩ	$T_A = 25°C$		1	5	mV
		$T_{AMIN} \leq T_A \leq T_{AMAX}$			6	mV
Input offset voltage adjustment range	$T_A = 25°C$, $V_S = \pm20$ V			±15		mV

Offset Voltage

FAIRCHILD
SEMICONDUCTOR®

LM741
Single Operational Amplifier

Features

- Short circuit protection
- Excellent temperature stability
- Internal frequency compensation
- High Input voltage range
- Null of offset

Description

The LM741 series are general purpose operational amplifiers. It is intended for a wide range of analog applications. The high gain and wide range of operating voltage provide superior performance in intergrator, summing amplifier, and general feedback applications.
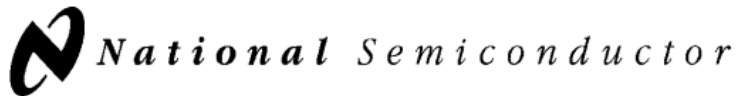
Electrical Characteristics

(V_{CC} = 15V, V_{EE} = - 15V. T_A = 25 °C, unless otherwise specified)

Parameter	Symbol	Conditions	LM741C/LM741I			Unit
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$	-	2.0	6.0	mV
		$R_S \leq 50\Omega$	-	-	-	
Input Offset Voltage Adjustment Range	$V_{IO(R)}$	V_{CC} = ±20V	-	±15	-	mV
Input Offset Current	I_{IO}	-	-	20	200	nA
Input Bias Current	I_{BIAS}	-	-	80	500	nA

# Offset Voltage

N *National Semiconductor*

LM741 Operational Amplifier

General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the co[mmon] ceeded, as well as freedom from [...]

The LM741C/LM741E are identi[cal] except that the LM741C/LM741[E are] guaranteed over a 0°C to +70[°C in-] stead of −55°C to +125°C.
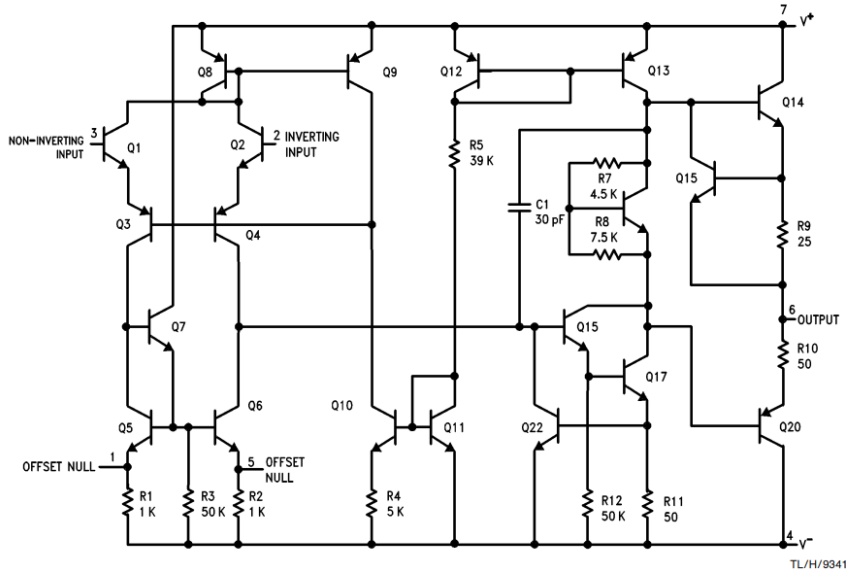
Offset Nulling Circuit

LM741   OUTPUT

10 kΩ

V−
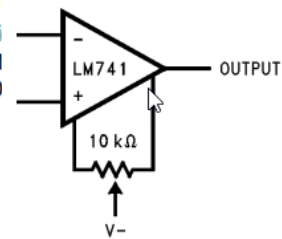
Electrical Characteristics (Note 3)

| Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$ $R_S \leq 10\ k\Omega$ $R_S \leq 50\Omega$		0.8	3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$ $R_S \leq 50\Omega$ $R_S \leq 10\ k\Omega$			4.0			6.0			7.5	mV mV
Average Input Offset Voltage Drift				15							μV/°C

Offset Voltage

Schematic Diagram

National

Schematic Diagram (Notes 5, 6)

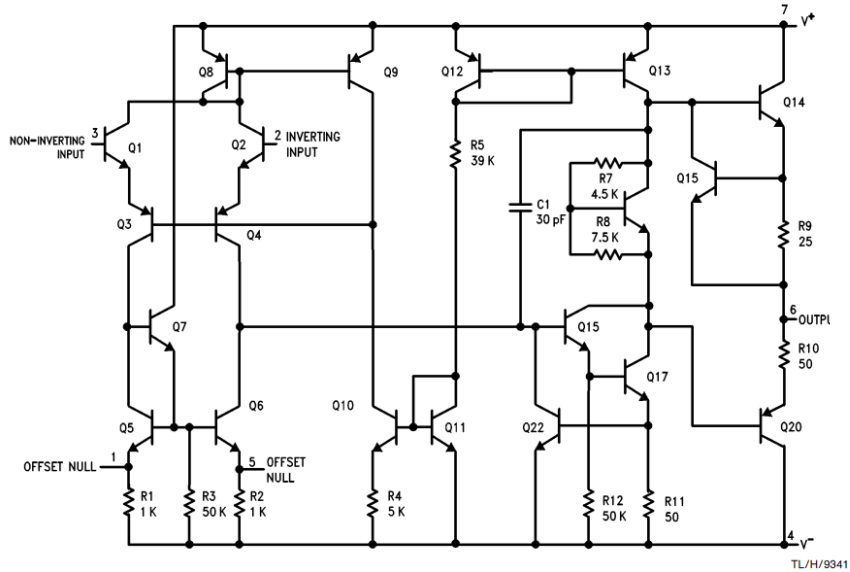CA741C, CA741, LM741C, LM741 AND FOR EACH AMPLIFIER OF THE CA1458, CA1558, AND LM1458
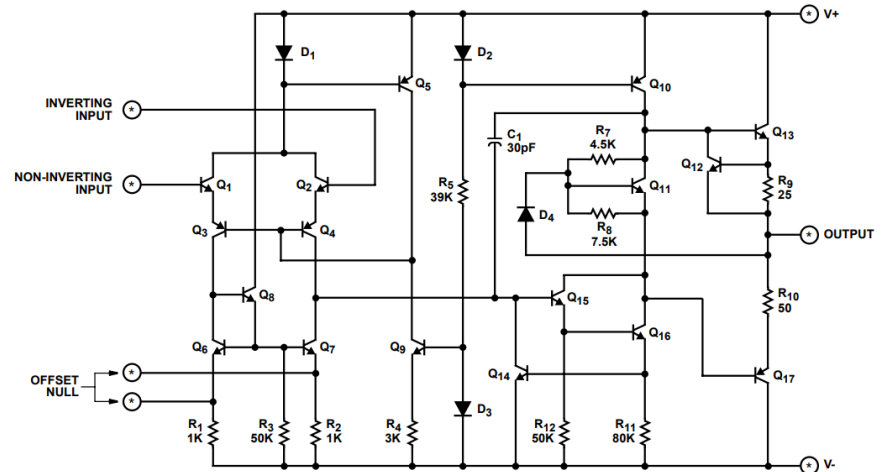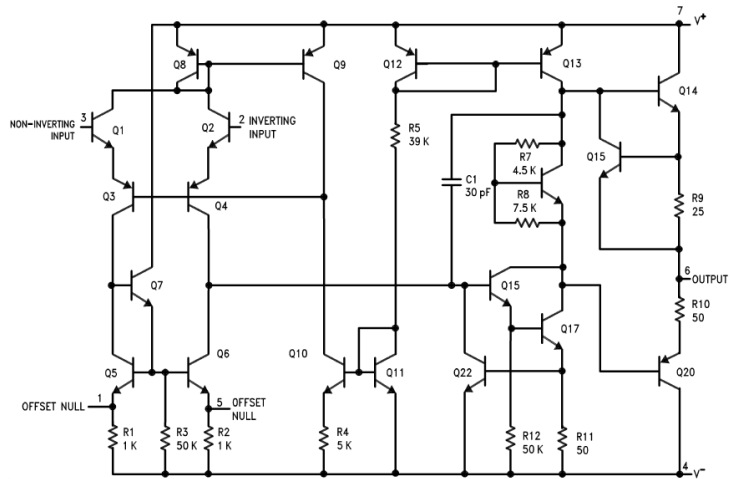

NOTES:

Intersil

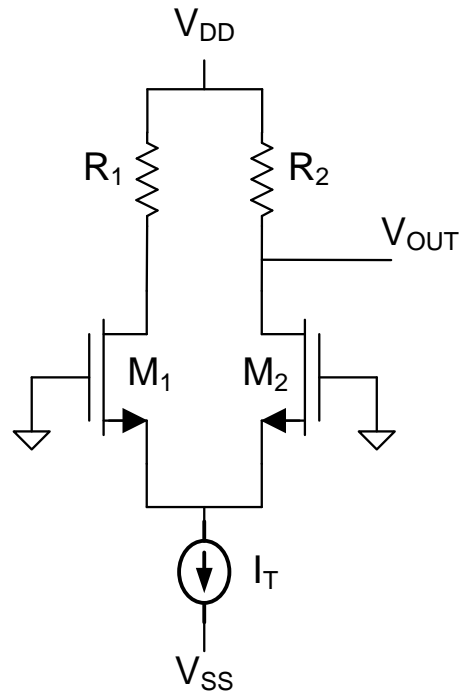# Offset Voltage

Schematic Diagram

National

7.2 Functional Block Diagram

Texas Instruments

Source of Random Offset Voltages

Consider as an example:

Ideally $R_1 = R_2 = R$, M_1 and M_2 are matched

$$V_{OUT} = V_{DD} - \left(\frac{I_T}{2}\right)R$$
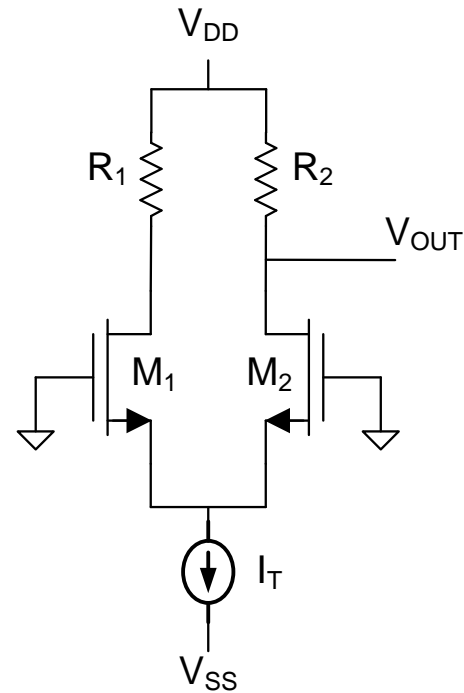
Assume this is the desired output voltage

Source of Random Offset Voltages

Consider as an example:

Ideally
 $R_1=R_2=R$
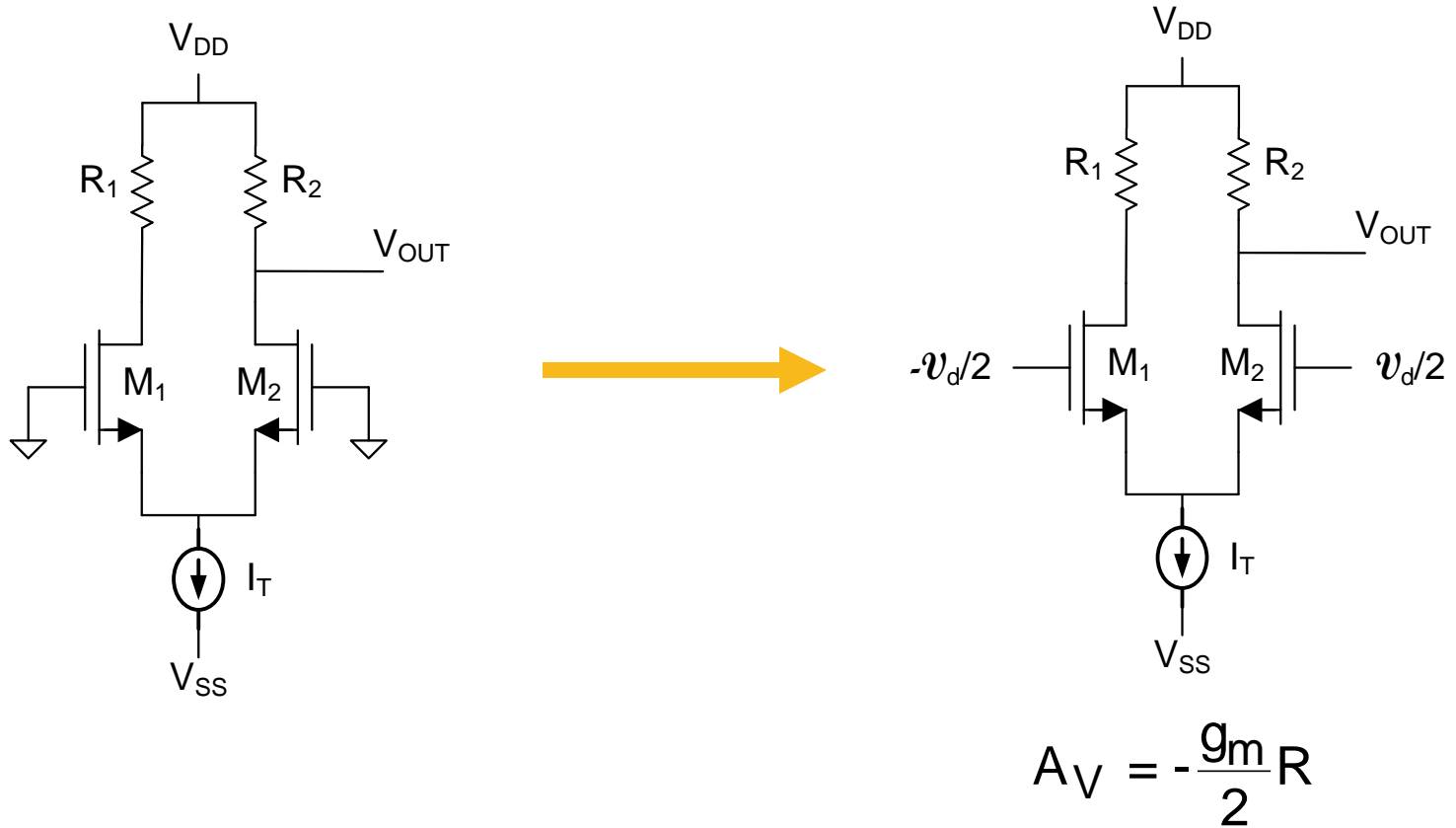 M_1 and M_2 matched

If everything ideal except $R_2=R+\Delta R$ (actually there will be mismatches between M_1 and M_2 also)

$$V_{OUT} = V_{DD} - \left(\frac{I_T}{2}\right)[R+\Delta R]$$
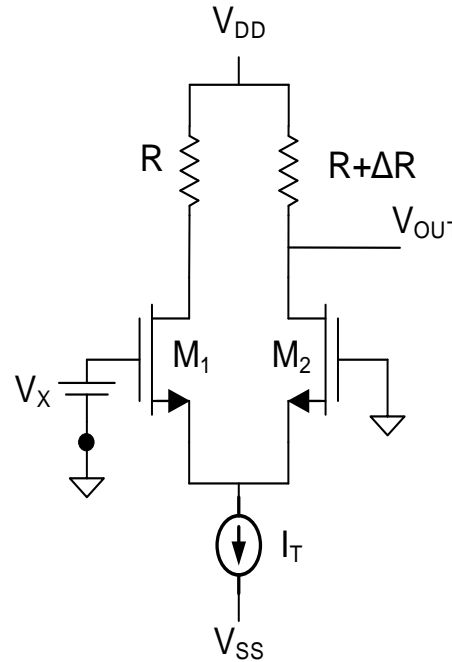
$$\Delta V_{OUT} = -\left(\frac{I_T}{2}\right)\Delta R$$

Source of Random Offset Voltages

Consider as an example:

$$A_V = -\frac{g_m}{2}R$$

Source of Random Offset Voltages

Determine the offset voltage – i.e. value of V_X needed to obtain desired output
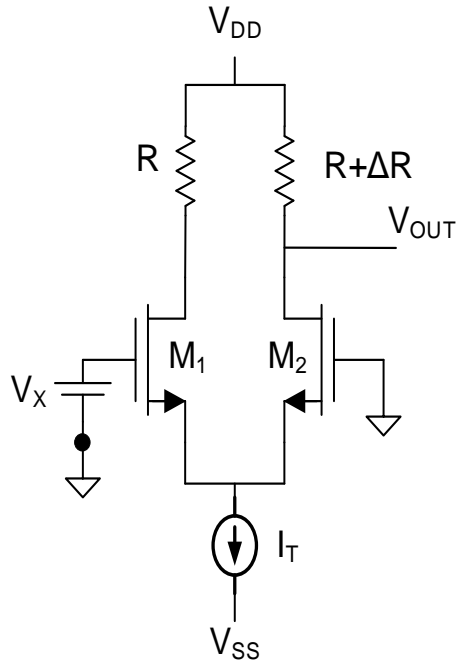

$$A_V = \frac{g_m}{2}R$$

$$V_{OUT} = \left[V_{DD} - \left(\frac{I_T}{2}\right)R \right] - \left(\frac{I_T}{2}\right)\Delta R + A_V V_X$$

To force V_{OUT} to its desired value of $\quad V_{OUT} = \left[V_{DD} - \left(\frac{I_T}{2}\right)R \right]$

$$V_X = \frac{1}{A_V}\left(\frac{I_T}{2}\right)\Delta R$$

Source of Random Offset Voltages

Determine the offset voltage – i.e. value of V_X needed to obtain desired output
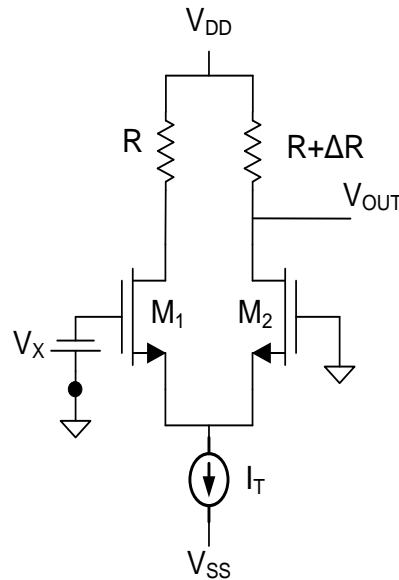

$$A_V = \frac{g_m}{2}R$$

$$V_X = \frac{1}{A_V}\left(\frac{I_T}{2}\right)\Delta R$$

$$V_X = \frac{2}{g_m R}\left(\frac{I_T}{2}\right)\Delta R = \left(\frac{I_T}{g_m}\right)\frac{\Delta R}{R} = \left(\frac{I_T}{I_T/V_{EB}}\right)\frac{\Delta R}{R} = V_{EB}\frac{\Delta R}{R}$$

$$V_X = V_{EB}\frac{\Delta R}{R}$$

Source of Random Offset Voltages

Determine the offset voltage – i.e. value of V_X needed to obtain desired output

$$A_V = \frac{g_m}{2}R$$

$$V_X = V_{EB}\frac{\Delta R}{R}$$

What can the designer do to reduce the offset voltage if the resistor value and statistics are fixed?
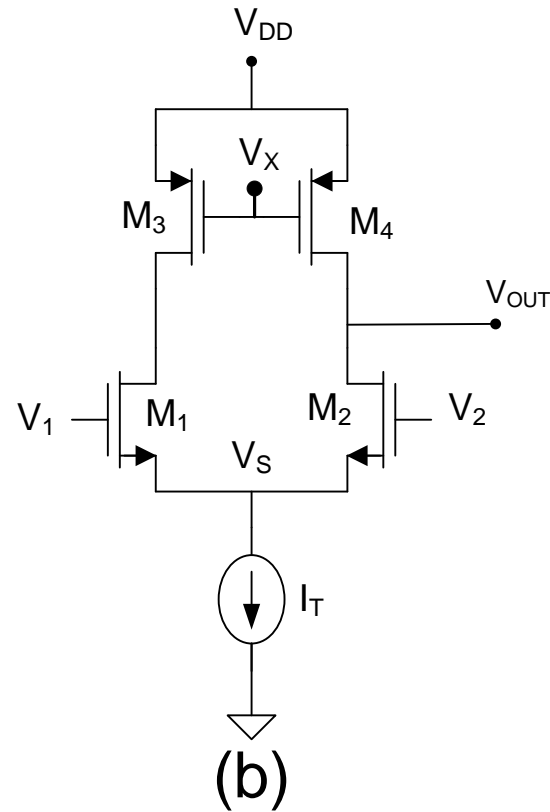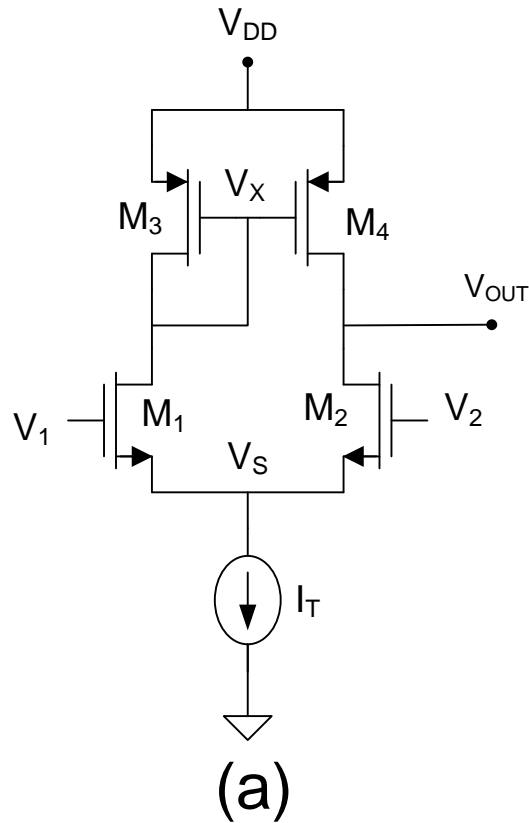
Reduce V_{EB}

Will that affect the voltage gain?

$$A_V = \frac{g_m}{2}R = \frac{2\frac{I_T}{2V_{EB}}}{2}R = \frac{1}{2V_{EB}}I_T R$$

Not if I_T is reduced by the same amount but that will affect signal swing and GB

Source of Random Offset Voltages

The random offset voltage is almost entirely that of the input stage in most op amps

(a)   (b)

Random Offset Voltage

- Due to random variations in process parameters and device dimensions

- Random offset is actually a random variable at the design level but deterministic after fabrication in any specific device

- Distribution naturally nearly Gaussian (could be un-naturally manipulated)

  Has zero mean

 Characterized by its standard deviation or variance

  Often strongly layout dependent

 Due to both local random variations and correlated gradient effects

  - o Will consider both effects separately
  - o Gradient effects usually dominate if not managed
  - o Good methods exist for driving gradient effects to small levels

Notation: Henceforth, the term "Random Offset" will refer to that due to local random variations and gradient effects will be considered separately

Offset Voltages due to Local Random Variations

Bulk   Source   Gate   Drain

n-channel MOSFET

Bulk   Source   Gate   Drain
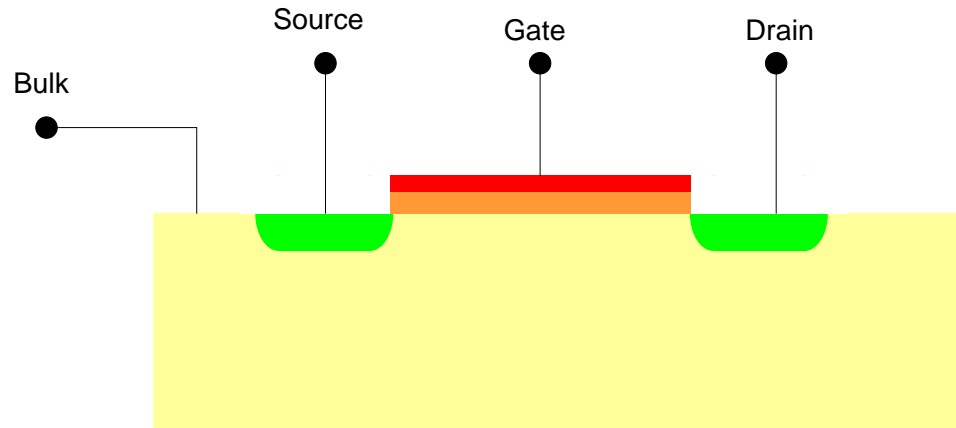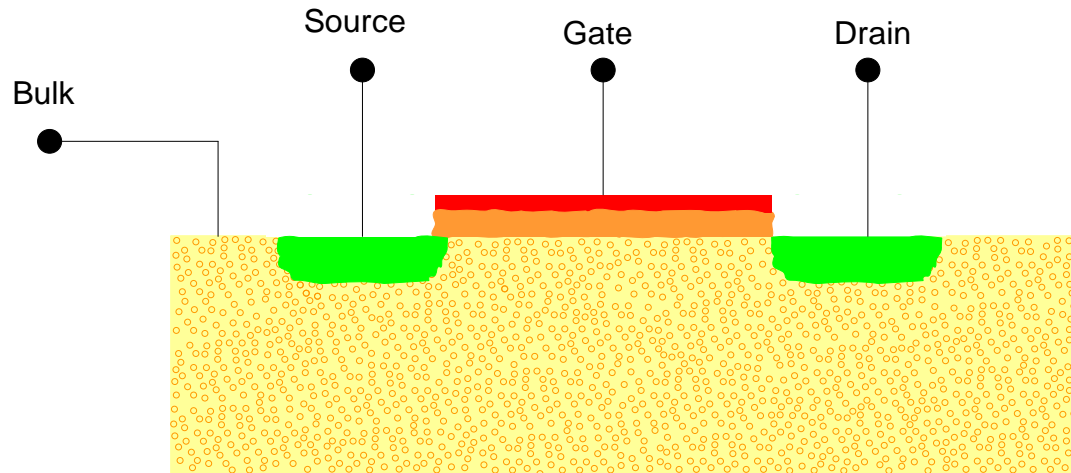
n-channel MOSFET

Impurities vary randomly with position as do edges of gate, oxide and diffusions

Model and design parameters vary throughout channel and thus the corresponding equivalent lumped model parameters will vary from device to device

Model Parameter Variation

Define p to be a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

If p(x,y) varies throughout a two-dimensional region, then
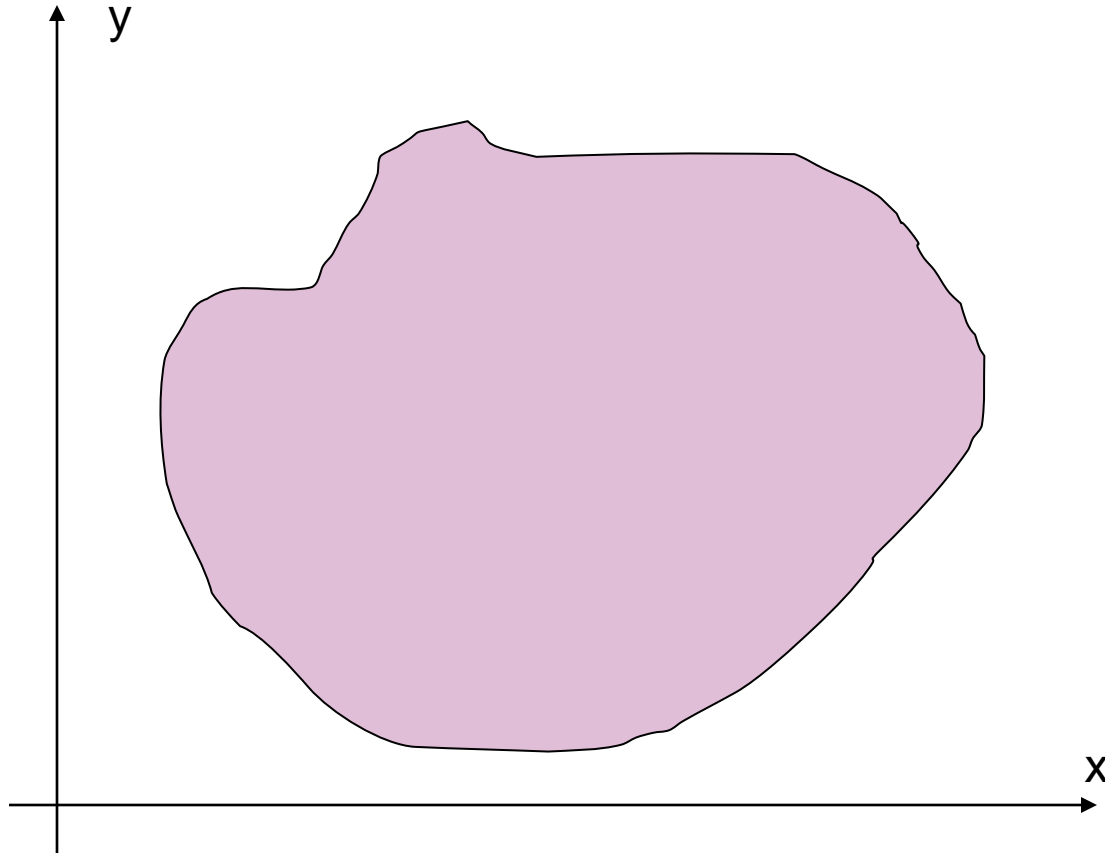
$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy$$

Parameters such at V_T, μ and C_{OX} vary throughout a two-dimensional region

Local random variations introduce a random component in device model parameters which are uncorrelated but for ideally matched devices they are identically distributed

e.g. $V_{TEQi} = V_{TN} + V_{TR\,i}$

V_{TRi} and V_{TRj} due to local random variations are uncorrelated for i≠j but if ideally matched they are identically distributed

Model Parameter Variation

$$p_{EQ} = \frac{1}{A} \int_A p(x,y)\,dx\,dy$$

Random Offset Voltages

The random offset associated with <u>local random variations</u> is due to mismatches in the four transistors, dominantly mismatches in the parameters $\{V_T, \mu, C_{OX}, W$ and $L\}$

The relative mismatch effects become more pronounced as devices become smaller

$$V_{Ti} = V_{TN} + V_{TRi}$$

$$C_{OXi} = C_{OXN} + C_{OXRi}$$
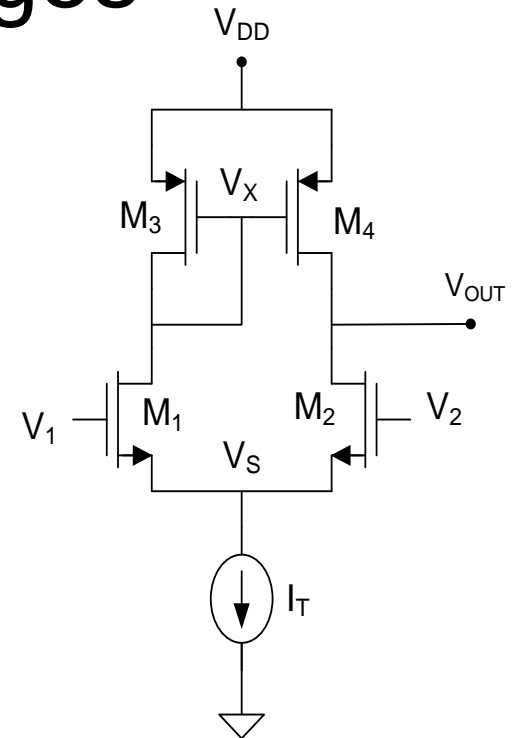
$$\mu_i = \mu_N + \mu_{Ri}$$

$$W_i = W_N + W_{Ri}$$

$$L_i = L_N + L_{Ri}$$

Each design and model parameter is comprised of a nominal part and a random component

It will be assumed that the random parts of each model parameter are uncorrelated but if ideally matched are identically distributed

(actually some small correlation in "model" parameters but will neglect in this course)

Random Offset Voltages

$V_{Ti}=V_{TN}+V_{TRi}$

$C_{OXi}=C_{OXN}+C_{OXRi}$

$\mu_i=\mu_N+\mu_{Ri}$

$W_i=W_N+W_{Ri}$

$L_i=L_N+L_{Ri}$

For each device, the device model is often expressed as

$$I_{Di} = \frac{(\mu_N + \mu_{Ri})(C_{OXN} + C_{OXRi})(W_N+W_{Ri})}{2(L_N +L_{Ri})}(V_{GSi}-(V_{TN} + V_{TRi}))^2 (1+(\lambda_N+\lambda_{Ri})[V_{DS}])$$

Because of the random components of the parameters in every device, matching from the left-half circuit to the right half-circuit is not perfect

This mismatch introduces an offset voltage which is a random variable

For this 4-transistor op amp, there are 24 uncorrelated random variables
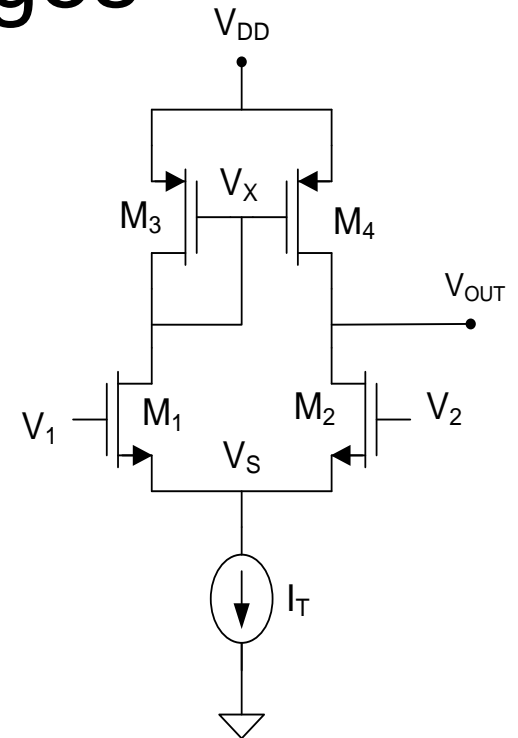
Random Offset Voltages

From a straightforward but tedious analysis (involving the 24 random variables) it follows that:

$$\sigma_{V_{OS}}^2 = 2\left[\frac{A_{VTO\,n}^2}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A_{VTO\,p}^2 + \frac{V_{EB\,n}^2}{4}\left(\frac{\frac{1}{W_n L_n}A_{\mu_n}^2 + \frac{1}{W_p L_p}A_{\mu_p}^2 + A_{COX}^2\left[\frac{1}{W_n L_n} + \frac{1}{W_p L_p}\right]}{+2A_L^2\left[\frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2}\right] + A_w^2\left[\frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2}\right]}\right)\right]$$

where the terms A_{VT0}, A_μ, A_{COX}, A_L, and A_W are process parameters

V_{DD}

$$A_{VT0} \cong \begin{cases} 21\,\text{mV}\cdot\mu & \text{(n-ch)} \\ 25\,\text{mV}\cdot\mu & \text{(p-ch)} \end{cases}$$
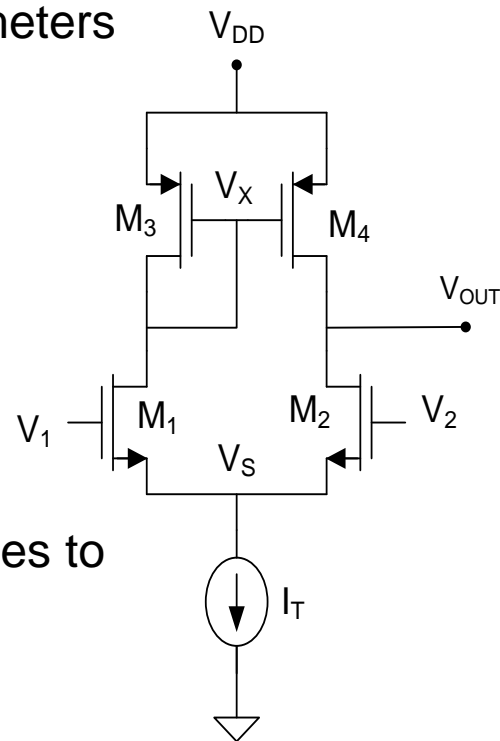
Typical values for matching
model parameters:

$$\sqrt{A_\mu^2 + A_{C_{OX}}^2} \cong \begin{cases} .016\mu & \text{(n-ch)} \\ .023\mu & \text{(p-ch)} \end{cases}$$

V_{OUT}

M_3 V_X M_4

$V_1 \dashv M_1$ $M_2 \vdash V_2$

V_S

$$A_L = A_W \cong 0.017\mu^{3/2}$$

Usually the A_{VT0} terms are dominant, thus the variance simplifies to

$$\sigma_{V_{OS}}^2 \cong 2\left[\frac{A_{VTO\,n}^2}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A_{VTO\,p}^2\right]$$

I_T

(Remember this is due to local random variations)

Random Offset Voltages

$$\sigma_{V_{OS}}^2 \cong 2\left[\frac{A_{VTOn}^2}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A_{VTOp}^2\right]$$

This expression has somewhat peculiar coefficients. The first term on the right is dependent upon the reciprocal of the area of the n-channel device but the corresponding coefficient on the second term on the right appears to depend upon the dimensions of both the n-channel and p-channel devices. But this can be rewritten as

$$\sigma_{V_{OS}}^2 \cong 2\left[\frac{A_{VTOn}^2}{W_n L_n} + \left(\frac{V_{EBn}}{V_{EBp}}\right)^2\frac{A_{VTOp}^2}{W_p L_p}\right]$$

The dependence of the variance on the area of the n-channel and p-channel devices is more apparent when written in this form.
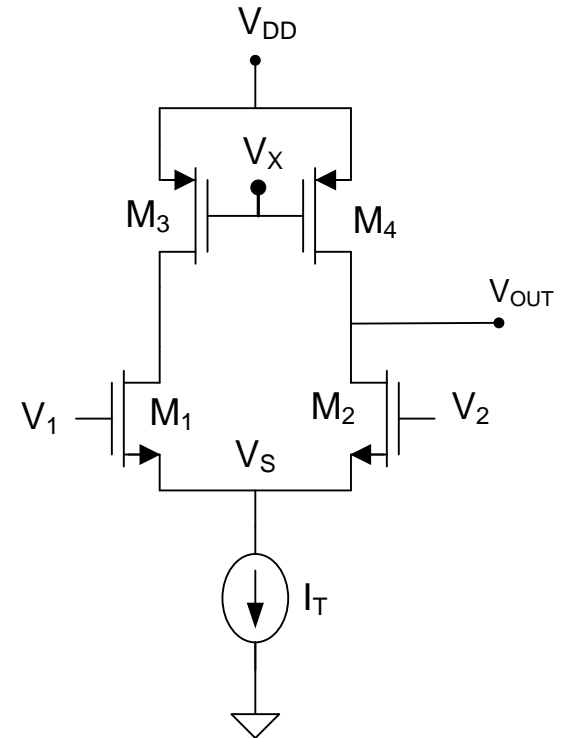
Random Offset Voltages

Correspondingly for differential output structure:

$$\sigma^2_{V_{OS}} = 2\left[\frac{A^2_{VTOn}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2} A^2_{VTOp} + \frac{V^2_{EBn}}{4}\left(\frac{1}{W_n L_n}A^2_{\mu_n} + \frac{1}{W_p L_p}A^2_{\mu_p} + A^2_{COX}\left[\frac{1}{W_n L_n} + \frac{1}{W_p L_p}\right] + 2A^2_L\left[\frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2}\right] + A^2_w\left[\frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2}\right]\right)\right]$$

which again simplifies to

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTOn}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A^2_{VTOp}\right]$$

Note these offset voltage expressions are identical!

Random Offset Voltages

Example: Determine the 3σ value of the input offset voltage for
The MOS differential amplifier if
a) M_1 and M_3 are minimum-sized and
b) the area of M_1 and M_3 are 100 times minimum size (with $L_n = L_p$)

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n\,L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n\,L^2_p}A^2_{VTO\,p}\right]$$
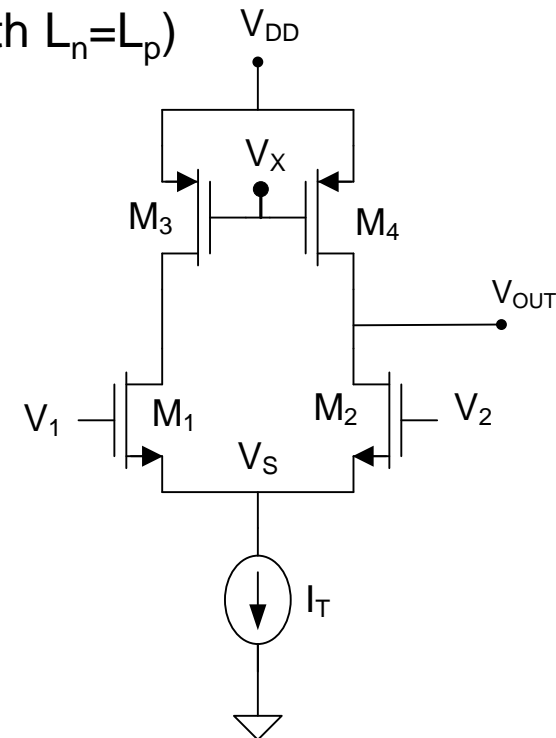
$$\sigma^2_{V_{OS}} \cong \frac{2}{W_n\,L_n}\left[A^2_{VTO\,n} + \frac{\mu_p}{\mu_n}A^2_{VTO\,p}\right]$$

a)

$$\sigma^2_{V_{OS}} \cong \frac{2}{(0.5\mu)^2}\left[.021^2 + \frac{1}{3}.025^2\right]$$

$$\sigma_{V_{OS}} \cong 72\text{mV}$$

$$3\,\sigma_{V_{OS}} \cong 216\text{mV}$$

Note this is a very large offset voltage !

Random Offset Voltages

Example: Determine the 3σ value of the input offset voltage for the MOS differential amplifier due to local random variations if:
a) M_1 and M_3 are minimum-sized and
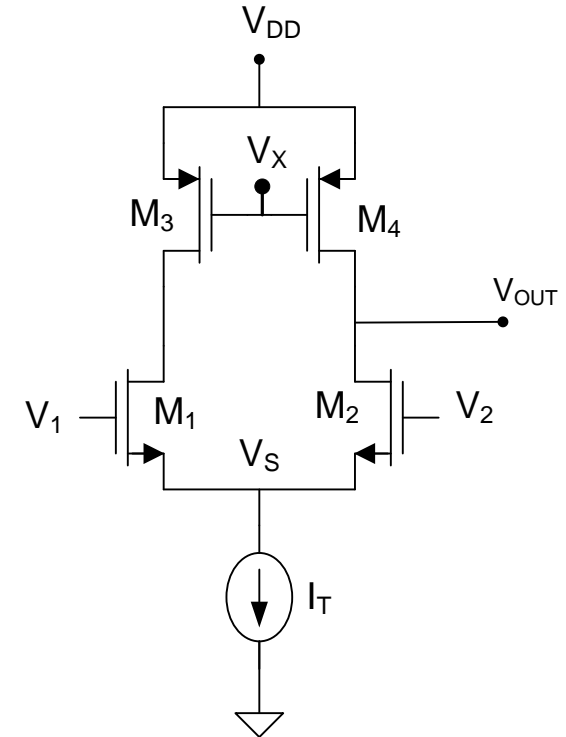b) the area of M_1 and M_3 are 100 times minimum size

$$\sigma_{V_{OS}}^2 \cong 2\left[\frac{A_{VTO\,n}^2}{W_n\,L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n\,L_p^2}A_{VTO\,p}^2\right]$$

$$\sigma_{V_{OS}}^2 \cong \frac{2}{W_n\,L_n}\left[A_{VTO\,n}^2 + \frac{\mu_p}{\mu_n}A_{VTO\,p}^2\right]$$

b)

$$\sigma_{V_{OS}}^2 \cong \frac{2}{100(0.5\mu)^2}\left[.021^2 + \frac{1}{3}.025^2\right]$$

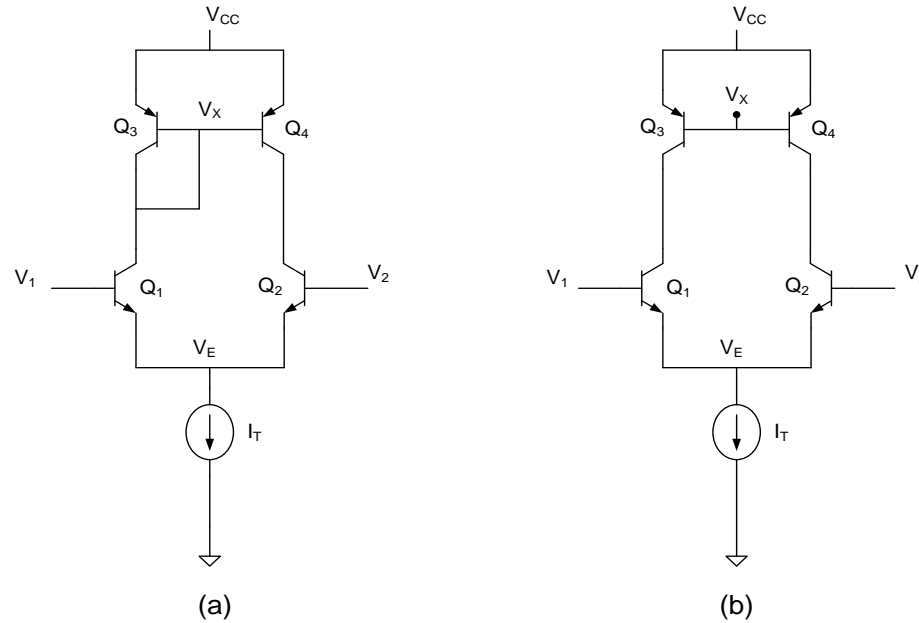$$\sigma_{V_{OS}} \cong 7.2\text{mV}$$

$$3\,\sigma_{V_{OS}} \cong 21.6\text{mV}$$

Note this is much lower but still a large offset voltage !

The area of M_1 and M_3 need to be very large to achieve a low offset voltage

Random Offset Voltages

(a)   (b)

It can be shown that

$$\sigma^2_{V_{OS}} \cong 2V_t^2 \left[\frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}} \right]$$

where very approximately
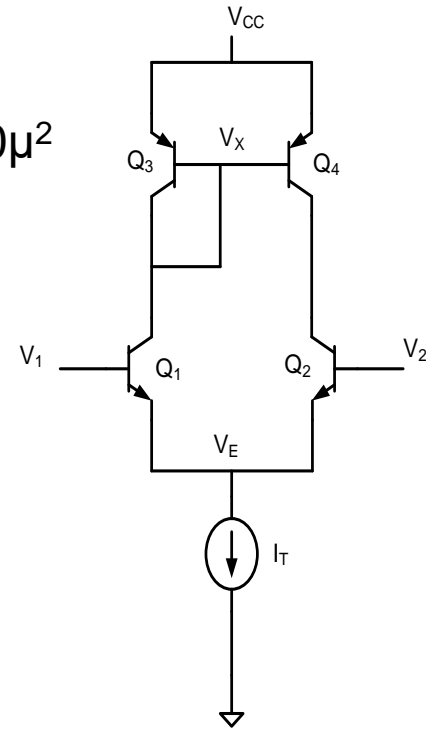
$$A_{Jn} = A_{Jp} = 0.1\mu$$

Random Offset Voltages

Example: Determine the 3σ value of the offset voltage of a the bipolar input stage due to local random variations if $A_{E1}=A_{E3}=10\mu^2$

$$\sigma^2_{V_{OS}} \cong 2V_t^2\left[\frac{A^2_{Jn}}{A_{En}}+\frac{A^2_{Jp}}{A_{Ep}}\right]$$

$$\sigma_{V_{OS}} \cong \sqrt{2}V_t\, A_J\,\frac{\sqrt{2}}{\sqrt{A_E}}$$

$$\sigma_{V_{OS}} \cong 2\bullet 25\text{mV}\bullet 0.1\mu\bullet\frac{1}{\sqrt{10\mu^2}}=1.6\text{mV}$$

$$3\sigma_{V_{OS}} \cong 4.7\text{mV}$$

Note this value is much smaller than that for the MOS input structure !

Random Offset Voltages

Typical offset voltages:

MOS - 5mV to 50MV
BJT -   0.5mV to 5mV

These can be scaled with extreme device dimensions

Often more practical to include offset-compensation circuitry

Stay Safe and Stay Healthy !

End of Lecture 22